

ABSTRACT

In modern sub-micron technologies with aggressive design rules, it is not always possible to have complete overlap of conductive lines with underlying vias. A process for manufacturing a semiconductor device having metal interconnects reduces or eliminates the recessing of metal in the vias, particularly when the metal in the vias is aluminum or an aluminum alloy. By manipulating the etch chemistry so that the etch rates of the aluminum alloy, the surrounding barrier metals, and the dielectric are comparable, it is possible to perform the metal over etch without forming voids in the exposed portion of the via. By eliminating the voids, thinning of the vias due to the presence of recesses is minimized, and electrical connections are less susceptible to electromigration. Consequently, device yield and reliability are increased.